WHAT IS CLAIMED IS:

1. A semiconductor package having a heat dissipating structure, comprising:

a substrate having a first surface and a second surface opposite to the first surface;

at least one chip mounted on the first surface of the substrate and electrically connected to the substrate;

a heat dissipating structure comprising a first heat sink and at least one second heat sink, wherein the first heat sink has at least one first positioning portion, and the second heat sink has at least one second positioning portion and at least one hollow portion, and wherein the second heat sink is mounted on the first surface of the substrate, and the first positioning portion of the first heat sink is mounted on the second positioning portion of the second heat sink, allowing the chip to be accommodated in a space defined by the first heat sink, the hollow portion of the second heat sink and the substrate; and

a plurality of solder balls mounted on the second surface of the substrate.

2. The semiconductor package of claim 1, wherein the first and second heat sinks are each shaped as a plate.

3. The semiconductor package of claim 1, wherein the first positioning portion is a flange, and the second positioning portion includes a flange and a recess.

4. The semiconductor package of claim 1, wherein first positioning portion is a recess, and the second positioning portion includes a flange and a recess.

5. The semiconductor package of claim 1, wherein the first and second positioning portions are respectively formed at peripheral regions of the first and second heat sinks.

6. The semiconductor package of claim 1, wherein peripheries of the first heat sink and the second heat sink are aligned with each other.

7. The semiconductor package of claim 1, wherein peripheries of the first heat sink and the second heat sink are arranged in a stagger manner.

8. The semiconductor package of claim 1, wherein when a plurality of the second heat sinks are provided, the second heat sinks are stacked on the substrate in a manner that peripheries of the second heat sinks are aligned with one another.

9. The semiconductor package of claim 1, wherein when a plurality of the second heat sinks are provided, the second heat sinks are stacked on the substrate such that peripheries of the second heat sinks are arranged in a stagger manner.

10. The semiconductor package of claim 1, wherein the first heat sink has a surface area larger than that of the second heat sink.

11. The semiconductor package of claim 1, wherein at least one additional heat sink is stacked on a side of the first heat sink free of contact with the second heat sink.

12. The semiconductor package of claim 11, wherein the additional heat sink has at least one hollow portion corresponding in position to the chip.

13. The semiconductor package of claim 1, wherein the heat dissipating structure further comprises a fan mounted on the first heat sink.

14. The semiconductor package of claim 1, wherein a plurality of slots are formed on a side of the second heat sink in contact with the substrate.

15. The semiconductor package of claim 14, wherein each of the slots has a stepped inner surface.

16. The semiconductor package of claim 14, wherein each of the slots has a tilted inner surface.

17. The semiconductor package of claim 1, wherein the chip is electrically connected to the first surface of the substrate via a plurality of solder bumps.

18. The semiconductor package of claim 17, further comprising an insulation material applied around the solder bumps.

19. The semiconductor package of claim 1, further comprising a thermal paste for adhering the first heat sink and the chip.

20. The semiconductor package of claim 1, further comprising an adhesion material filled between the second heat sink and the first surface of the substrate.